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(12) **United States Patent**  
**Chen**(10) **Patent No.:** **US 6,717,847 B2**  
(45) **Date of Patent:** **\*Apr. 6, 2004**(54) **SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE**

## FOREIGN PATENT DOCUMENTS

JP 8171515 7/1996  
WO WO09518407 7/1995(75) Inventor: **Jian Chen**, San Jose, CA (US)

## OTHER PUBLICATIONS

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/229,258**(22) Filed: **Aug. 26, 2002**(65) **Prior Publication Data**

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**Related U.S. Application Data**

(63) Continuation of application No. 09/956,340, filed on Sep. 17, 2001, now Pat. No. 6,456,528.

(51) **Int. Cl.**<sup>7</sup> ..... **G11C 16/04**(52) **U.S. Cl.** ..... **365/185.03; 365/185.24**(58) **Field of Search** ..... 365/185.03, 185.12, 365/185.24, 230.03, 184(56) **References Cited****U.S. PATENT DOCUMENTS**

5,043,940 A	8/1991	Harari
5,095,344 A	3/1992	Harari
5,172,338 A	12/1992	Mehrotra et al.
5,187,338 A	2/1993	Kaigler
5,287,478 A	2/1994	Johnston et al.
5,297,148 A	3/1994	Harari et al.
5,313,585 A	5/1994	Jeffries et al.
5,359,569 A	10/1994	Fujita et al.

(List continued on next page.)

International Search Report from corresponding PCT case PCT/US02/29177, PCT Searching Authority Feb. 4, 2003, 4 pages.

Anand, M.B., et al., "NURA: A Feasible Gas-Dielectric Interconnect Process," *1996 Symposium on VLSI Technology Digest of Technical Papers*, pp. 82-83.Zhao, B., et al., "Reliability and Electrical Properties of New Low Dielectric Constant Interlevel Dielectrics for High Performance ULSI Interconnect," *IEEE*, pp. 156-163 (1996).Choi, J.D., et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling-Down and Zero Program Disturbance," *1996 Symposium on VLSI Technology Digest of Technical Papers*, pp. 238-239.Aritone, S., et al., "A 0.67 $\mu$ m<sup>2</sup> Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell) for 3V-only 256Mbit NAND EEPROMs," *IEDM Technical Digest*, pp. 61-64 (1994).

(List continued on next page.)

*Primary Examiner*—Thong Q. Le(74) *Attorney, Agent, or Firm*—Parsons Hsue & de Runtz LLP(57) **ABSTRACT**

A flash non-volatile memory system that normally operates its memory cells in multiple storage states is provided with the ability to operate some selected or all of its memory cell blocks in two states instead. The two states are selected to be the furthest separated of the multiple states, thereby providing an increased margin during two state operation. This allows faster programming and a longer operational life of the memory cells being operated in two states when it is more desirable to have these advantages than the increased density of data storage that multi-state operation provides.

**14 Claims, 7 Drawing Sheets**